Dhruv Baronia

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Portfolio: https://dhruvbaronia.com
Github: github.com/boronhub

Education

- **University of Illinois at Urbana-Champaign** — Urbana, Illinois
  Masters of Science - Computer Science — *August 2024 - May 2026*
  Advisor: *Prof. Vikram Adve*

- **University of Illinois at Urbana-Champaign** — Urbana, Illinois
  Bachelor of Science - Computer Science and Linguistics — *August 2021 - May 2024*
  Courses: *Parallel Programming (CS 483), ML for Compilers and Architecture (CS 598), Computer Systems Engineering (ECE 391), Algorithms & Models of Computation (CS 374), Programming Languages and Compilers (CS 421), Program Verification (CS 476), Advanced Compiler Construction (CS 526),*
  Extracurriculars: *SIGPwny (Cybersecurity club); Intro to C++ - Course Assistant, Crossword Club - Treasurer, PizzaFM(College Radio) - DJ and Staff Writer, The Daily Illini (School newspaper) - Staff Writer*
  GPA: *3.6/4.0*

Skills Summary

- **Languages**: C++, C, Python, Rust, Racket, Dart, Bash, Haskell, Java, JavaScript, OCaml
- **Frameworks**: LLVM, MLIR, XLA, ONNX, TensorFlow, PyTorch, Django, Flask, NodeJS, Flutter
- **Tools**: Linux, CMake, PyTest, Catch2, AWS, GCP, Grafana, Prometheus, Docker, git, PostgreSQL, MongoDB, ZMQ

Experience

- **Cadence Design Systems** — Austin, TX
  Compiler Engineering Intern — *May- Aug 2023, 2024*
  - **MLIR**: Conversion passes for lowering 20+ ML operations to optimized library calls
  - **Constant Handling**: Implemented handling for raw constant data parsed from ONNX files and loading it into a JIT pipeline for optimziation
  - **Glow**: Modified Glow internals to generate end-to-end tests using custom ops
- **Advanced Micro Devices, Inc. (AMD)** — San Jose, CA
  Compiler Engineering Intern — *May 2022 - Aug 2022*
  - **MLIR**: Writing MLIR passes for various internal dialects and developing a new graph-based dialect. Created a new dialect for lowering logical graph representation to hardware level
  - **Memory Allocation**: Worked on scheme for memory allocation and routing on AIE devices
  - **ML Compilers**: Gained experience on the flow for ML compilers, from understanding various ops at the IR level to how we can optimize them at the hardware level
- **LLVM Research Group at UIUC** — Urbana, IL
  Research Intern — *Feb 2022 - Present*
  - **Undergraduate Research**: Actively working on various compiler related projects under Prof. Vikram Adve
  - **Heterogenous Compilers**: Wrote several tests and passes for the release for Heterogeneous Parallel Virtual Machine (HPVM) tool
  - **ASPLOS'24 Paper:** : Hydride: A Retargetable and Extensible Synthesis-based Compiler for Modern Hardware Architectures
    - Ported HPC benchmarks to Halide
    - Integrated external libraries for x86 fuzzer tests
    - Worked on code synthesis using a Racket DSL
    - Set up build system for project using Makefiles and Python scripts
  - **Tensor Extensions to LLVM**: Working on XLA frontend for retargetable tensor code generation framework for LLVM (TLX)

Projects

- **Rust MIR Pass - Rust**: Analysis passes for Rust mid-level IR (MIR)
- **charhead - C++, LLVM**: JIT Compiler using LLVM for custom stack-based esoteric language
- **mips-emu - Rust, MIPS**: MIPS emulator written in Rust
- **torch-sat - PyTorch, Z3**: Checking correctness of fusion optimizations in PyTorch graphs using an SMT sovler
- **gpt3-dart - Dart, API**: Dart bindings for OpenAI's GPT-3 API, Featured on their official page. Used across 50+ Flutter projects
- **shiritor.io - React, Flask, WebSockets**: Online version of popular word game. Worked on developing the frontend and in-game mechanics